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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,612	12/31/2001	Howard S. David	42390.P13874	2520

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EXAMINER

LI, ZHUO H

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 09/16/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/039,612

Applicant(s)

DAVID, HOWARD S.

Examiner

Zhuo H Li

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of "cache line divided into two segments" which is claimed in claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Page 6 lines 4-5, "the DRAM is placed on a motherboard rather that on a memory module" should be -- the DRAM is placed on a motherboard rather than on a memory module--.

Appropriate correction is required.

Claim Objections

3. Claims 2, 7 and 11 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to

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cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Saulsbury discloses an apparatus (100, figure 1) comprising an array, i.e., primary data cache bank tag/flag storage, (148, figure 2) of tag address storage locations (col. 7 lines 42-61), and a command sequencer and serializer unit, i.e., primary data cache bank logic, (150, figure 2) coupled to the array of tag address storage locations (figure 2), the command sequencer and serialize unit to control a data cache associated with a memory module, i.e., primary data cache bank N (122, figure 2), each tag address storage location in the array of tag address storage locations corresponding to a cache line, i.e., cache line 0 and cache line 1 (figure 2) divided into two segments (col. 7 lines 21-61).

Regarding claim 2, Saulsbury discloses the apparatus wherein the segmentation of the cache lines is an optional feature (col. 7 lines 21-40).

Regarding claim 3, Saulsbury discloses the apparatus further comprising a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage

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locations corresponding to one of a plurality of memory modules, i.e., each tag identifies the row in the corresponding memory bank 118, (col. 7 lines 41-61).

Regarding claims 4-5, Saulsbury discloses each of the plurality of arrays of tag address storage locations organized into a plurality of ways and 4 ways (col. 3 lines 54-63).

Regarding claim 6, Saulsbury discloses an apparatus (100, figure 1) comprising a memory device (118, figure 2) and a data cache, i.e., primary data cache storage (144, figure 2) couple to the memory device, i.e., couple together via the cache line bus 4096 (figure 2), the data cache controlled by commands delivered by a memory controller, i.e., data cache bank logic (150, figure 2) component over a memory bus, i.e., cache line 4096 bus and control bus, (figure 2), the memory controller component including an array of tag address storage locations, i.e., data cache bank address/tag comparison circuit, (154, figure 5), each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments, i.e., data cache bank address/tag comparison circuit sends commands to and receives commands from the data cache bank tag/flag storage which indicate which corresponding cache line is dirty and/or hit/miss the request, (col. 7 lines 21-61 and col. 9 line 54 through col. 10 line 40).

Regarding claim 7, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claims 8-9, the limitations of the claims are rejected as the same reasons set forth in claims 4-5.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westberg (US PAT. 5,361,391) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 10, Westberg discloses a system (10, figure 1) comprising a processor (12, figure 1), a memory controller (14, figure 1) couple to the processor (col. 3 lines 35-48), the memory controller including an array of tag address storage locations (30a and 30b, figure 2, and col. 4 lines 34-46) and a command sequencer and serializer unit, i.e., cache control logic, couple to the array of the tag address storage locations (col. 4 lines 34-59), and a memory module (16, figure 2) couple to the memory controller via the address, data and control buses. Westberg differs from the claimed invention in not specifically teaches the memory module including a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of the tag address storage locations corresponding to a cache line divided into two segments.

However, Saulsbury teaches the memory module, i.e., memory block (104, figure 2) including a memory device, i.e., memory bank (118, figure 2), and a data cache, i.e., primary data cache (122, figure 2), and the data cache is coupled to the memory device via the cache line bus 4096, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments (col. 7 lines 21-61 and col. 9 line 54 through col. 10 line 40).

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Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Westberg in having a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of the tag address storage locations corresponding to a cache line divided into two segments, as per teaching by the memory module of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claims 13-14, the limitations of the claims are rejected as the same reasons set forth in claims 4-5.

Regarding claim 15, Westburg discloses a point-to-point interconnect to coupled the memory controller to the memory module (figure 2, and col. 3 line 55 through col. 4 line 10).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McAllister et al. (US PAT. 6,463,506) discloses arrangement of data within cache lines so that tags first data received (abstract).

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9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

September 4, 2003


MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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